ECE 4530 - Final Project Report for a FMCW Radar Transceiver

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We present a design for a Frequency Modulated Continuous Wave (FMCW) Radar Transceiver for use in distance-ranging applications with operating frequencies between 25 and 30 GHz. The goal is to deliver 10 dBm of power on the transmitter side and accept a minimum of -20 dBm on the receiver side. The use of 50Ω source and load impedances is assumed for matched antennas of a 50Ω system. Our design is tested in simulation via Cadence Virtuoso ADE, satisfying input and output power specifications, as well as mixing capabilities.

I. INTRODUCTION & MOTIVATIONS

For our project, we aimed to implement a duplex FMCW radar transceiver. Our group is interested in this project because we hope to learn more about RF design through implementing most of the blocks that comprise a transceiver and would specifically like to focus on reducing the effect of the transmit to receive direct communication path.

Frequency Modulated Continous Wave Radar is a radar scheme that relies on transmitting a continuous signal with frequency modulation over time. One example of frequency modulation that is used is a chirp signal, where the local oscillator's frequency over time follows a sawtooth pattern. This signal bounces off an object to be imaged, and the reflected signal is received. This reflection takes time, and by the time the reflected signal has been received, the local oscillator is at a different frequency. The difference of these frequencies can be measured and used to calculate the distance from the object to the radar. One of the advantages of this form of radar is that by using a mixer to generate a signal at the difference between the received and transmitted signals, the following stages operate at much lower frequencies, which makes them easier to design. A disadvantage of this form of radar is that since the transmit and receive frequencies can be so close, it is difficult to filter them out from each other, and leakage from transmit to receive becomes a much bigger problem. Our design attempts to implement this radar scheme and address the problem of transmit to receive leakage. We have centered our design around a low range, high accuracy application such as medical imaging, as it allows us to relax our output power requirement but requires a high operating frequency range with large bandwidth.

II. PRINCIPLES OF OPERATION

The connection of the different system components can be seen in the high level diagram, Fig. 2. The Oscillator is an off chip device that supplies a single ended frequency modulated chirp from 25 GHz to 30 GHz to the power amplifier with a low voltage amplitude and low power. The power amplifier amplifies the power of the oscillator in order to drive the transmitter antenna at 10 dBm. The power amplifier also provides two amplified oscillator signals 180 degrees out of phase to drive the mixer LO transistors. Lastly on the transmitter path, the delay line time-shifts and attenuates the power amplifier signal to create a signal seen at the receiving antenna, taking into account the delay time and free space loss for a fixed separation distance of and assuming perfectly matched hertzian dipole antennas. On the receiving side, the LNA takes in the reflected signal with a minimum power of -20 dBm and amplifies it for reception by the mixer. The mixer takes in the LNA signal and down-converts the frequency to between 0 GHz and 5 GHz. The output is then the difference in frequency between the output and reflected signal. This is sent to an off chip analog to digital converter for processing and distance calculation.

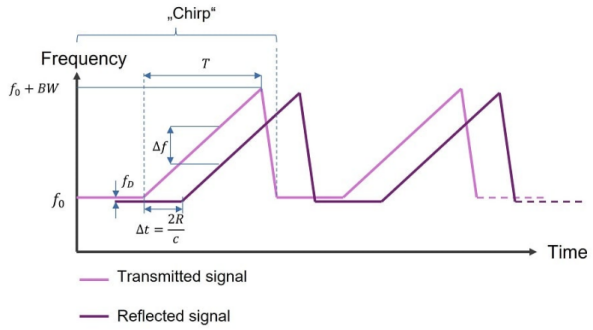

FIG. 1. **FMCW Theory of Operation** This diagram shows the theory behind FMCW radar, where the current transmitted frequency is compared to the reflected signal frequency in order to calculate the travelled distance. Image source: https://www.renesas.com/us/en/blogs/basics-fmcw-radar

III. KEY SPECIFICATIONS

TABLE I. Key Design Specifications

Specification	Desired	Achieved
Transmit/Receive Frequency Range	25GHz-30GHz	25GHz-30GHz
Output Power	>10dBm	10.1dBm
Input Power (minimum)	-20dBm	-20dBm
Noise Figure	<10dB	29.5dB
Pdc	<200mW	186mW
Supply Voltage	<3V	2.5V

The key specifications can be found in Table I. These specifications are driven by our application, which requires a high

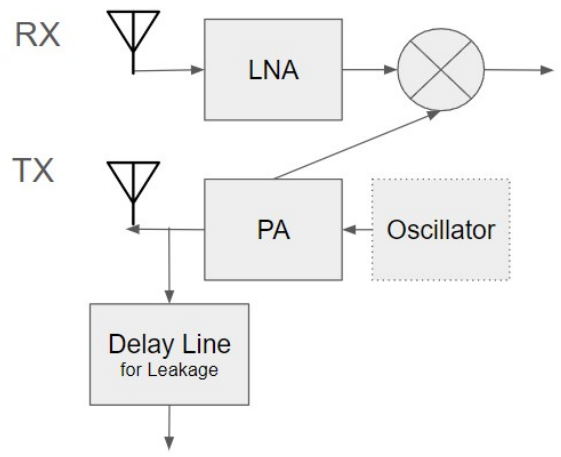

FIG. 2. **High Level Diagram of Transceiver** The receiver path is on the top and includes the LNA and the mixer. The transmitter path is on the bottom and includes the local oscillator, Power Amplifier, and the delay line

frequency range in order to have high measurement accuracy, and a power level of 10dBm in order to have our required range.

IV. MODULE DESIGN

Each member of our team was responsible for one primary module, although we collaborated in understanding, designing, implementing, and interfacing our designs. Each of the following sections go into more detail about each of the modules, the Low Noise Amplifier (Elizabeth Polito), the Power Amplifier (Christopher Lonergan), and the Mixer (Jeffrey Wilcox). Additionally, Christopher Longergan researched and developed a delay line for use in leakage cancellation between the Low Noise Amplifier and the Power Amplifier.

A. Low Noise Amplifier Design

The Low-Noise Amplifier (LNA) is the first element of the receive chain in the proposed design. Its primary purpose is to amplify the received FMCW signal, which is significantly attenuated compared to the transmitted signal (specified as -20dBm with a 50 Ohm source impedance), with enough gain in a single stage to mask the noise added by future stages. The importance of having a low-noise, high-gain first amplifying stage in a receiver is evident from Friis' formula, given as:[1]

$$\mathrm{F}_{total} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_{a,1}} + \frac{F_3 - 1}{G_{a,1}G_{a,2}} + \ldots$$

In this equation, F_n is the noise factor of stage n and $G_{a,n}$ is the gain provided by stage n. Thus, a large $G_{a,1}$ and small F_1 minimize our noise factor overall.

TABLE II. LNA Specifications

Specification	Desired	Achieved
Transmit/Receive Frequency Range	25GHz-30GHz	25GHz-30GHz
Gain Over Band	9-12dB	9.925dB
Gain Ripple Over Band	<3dB	0.9dB
Power	<10mW	6.5mW
NF	10dB	10.9dB

Various topologies for the LNA were considered, including single-transistor and cascode-based designs, but ultimately an inverter-based topology was selected due to its ability to provide a high gain and achieve the desired bandwidth while contributing minimally to SNR degradation. An inverter with resistive feedback works well as an LNA and provides gain on the order of $g_m R_f$ with

$$\mathrm{F} \approx 1 + \frac{\gamma}{(g_{mn} + g_{mp})R_s}$$

Furthermore, research was conducted to determine methods to extend the gain and bandwidth of an inverter-based LNA. One such method, inductive peaking, and allows for the bandwidth to be extended through the incorporation of an inductor between the RF input and gate of the bottom NMOS[2], as shown in Figure 3. The inverter itself ideally does not contribute as a noise source as it is a passive component so the design works well as an LNA. This topology introduces complex conjugate poles at $(\sqrt{LC_{gs}})^{-1}$ which allows the bandwidth to be extended compared to the basic resistive-feedback inverter.

The primary challenges faced while implementing this topology were the use of real models for inductive components and interfacing between the LNA and mixer. For the inductor, a gpdk045 model was used, which introduced significant parasitics and required adjustment of the values of all components since its Q appeared to be decreased significantly. In an improved design, a more optimal inductor would be used to take advantage of the benefits of the topology. Next, to address the challenge of interfacing with the mixer, we initially considered the use of a very large decoupling capacitor. However, we decided to employ a buffer stage instead as the capacitor needed was unreasonably large. The final solution introduced a pole due to the buffer stage, but still meets spec in the 25-30 GHz range. To improve upon this design, a matching network could be design to optimally translate between the stages with maximum power transfer.

B. Power Amplifier Design

The Power Amplifier (PA) is designed to accept a 50mV signal from the off-chip local oscillator and amplify it to drive 2V peak-to-peak onto the transmit antenna, which we model as an ideal 50 Ohm resistor. It is also required to generate a

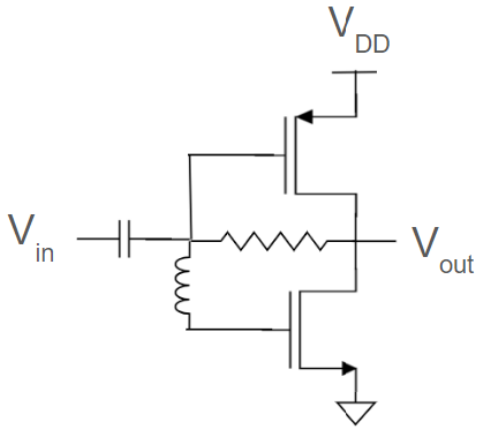

FIG. 3. **LNA Topology** The Low Noise Amplifier consists primarily of a CMOS inverter to provide high gain with an inductive peaking technique.

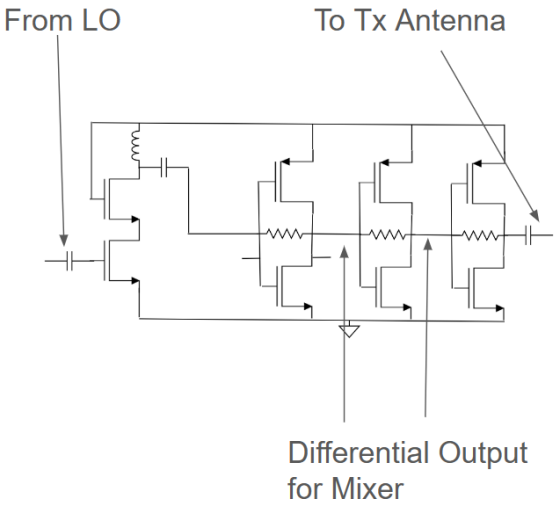

FIG. 4. **Power Amplifier Topology** The Power Amplifier consists of an inductively loaded common source stage, followed by three CMOS inverters. The input and output of the second CMOS inverter stage is used as the differential input of the mixer.

high amplitude differential signal for use in the mixer. A tabulation of specifications and achieved performance can be seen in Table. III. Several topologies were explored in the design of this module. In order to achieve high gain, we first considered using a topology such as a 2-stage OTA using a differential pair, a common source stage, and cascoding to increase gain. However, after implementing that topology, it became apparent that it would not be able to meet the bandwidth requirements due to the amount of low-frequency poles present in a typical OTA implementation. The next topology considered was a multistage CMOS inverter cascade. This topology presents the benefit of supporting a high bandwidth as well as providing high gain. However, we ultimately decided on a topology featuring 4 stages that can be seen in Fig. 4. The first stage is an inductively loaded common source amplifier used to provide gain at high BW, as the inductor resonates out the large parasitic capacitance seen by the first stage's output. The following stages are CMOS inverters, but they serve different purposes. The first CMOS inverter following the common source stage is used to provide gain. The second CMOS inverter is used to provide near unity gain to generate a high amplitude differential output for the mixer. The final CMOS inverter is a driver stage made of large transistors in order to drive the 50 Ohm load. Large width transistors are necessary so that $r_o//50$ is large enough that the stage does not attenuate too much, and so that the output impedance of the stage is much lower than 50.

The primary challenge with implementing this was juggling driving the 50 Ohm load while providing high gain at high bandwidth and being loaded by the mixer on an inner stage. Each piece was very hard to separate from the rest, and it led to a design process that was harder to subdivide. In addition, meeting the power spec was difficult, as transistors had to be very large on the driver stage in order to have a low enough output impedance with gain to drive the 50 Ohm load.

TABLE III. Power Amplifier Specifications

Specification	Desired	Achieved
Transmit/Receive Frequency Range	25GHz-30GHz	25GHz-30GHz
Min. Gain Over Band	30dB	31.29dB
Min. Output Power (50 Ohm Load)	10mW	10.1mW
Gain Ripple Over Band	<3dB	2.71dB
Power	<200mW	177mW

C. Mixer Design

The job of the mixer is to act as a voltage multiplier which for two different single frequency pure sinusoids results in two pure sinusoids whose frequencies are the sum and the difference of the input frequencies. To achieve this, two transistor gates are controlled by 180 degree phase shifted inputs allowing signal to pass through one at a time. Ideally, one will be on for half of the control signal or LO (local oscillator) signal period while the other is off and then off for the other half of the period while the other one is on. Differential mixers reduce the feedthrough frequency magnitude, the primary reason we decided to use a differential output. Initial research revealed two primary considerations for mixer topologies. The first is whether the mixer is single or double balanced. In a single balanced mixer, the input is not differential, whereas the input is differential in a double balanced mixer. Double balanced mixers generate less even order harmonic distortion whereas single balanced mixers exhibit less input-referred noise[1]. A double balanced mixer was decided on to reduce less even order harmonic distortion although the mixer would have more of an impact on the noise figure.

The second consideration is whether to use an active or pas-

TABLE IV. Mixer Specifications

Specification	Desired	Achieved
Transmit/Receive Frequency Range	25GHz-30GHz	25GHz-30GHz
Conversion Gain	> 0 dB	0 dB

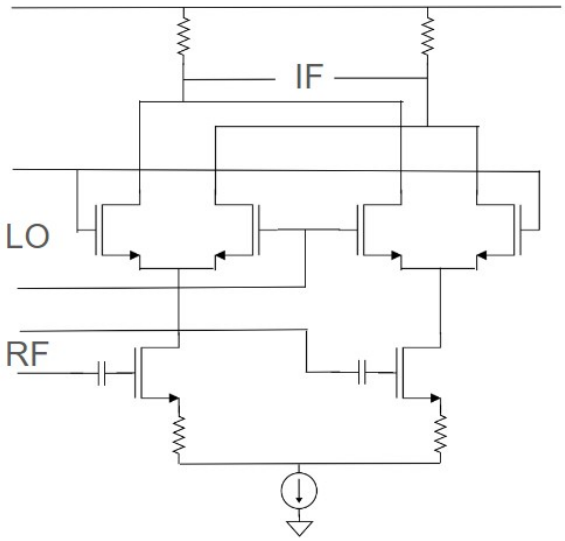

FIG. 5. **Gilbert Cell with Degenerated Input Transistors** This diagram shows a modified Gilbert Cell with degenerated transistors for higher input impedance

sive mixer. We decided to use an active mixer to prevent signal degradation and reduce the gain needed from an IF amplifier. Due to the need for higher input impedance at operation frequency, degeneration resistors were added to the input transistors which reduced the gain of the mixer in exchange for better matching between the LNA and the mixer. Besides the degeneration resistors, the topology was that of a classic Gilbert Cell.

The design was primarily driven by obtaining good conversion gain considering the LO transistors as cascodes meaning they can do not affect the conversion gain as the impedance looking into the LO drain is much greater than the load resistor. Therefore the conversion gain is $A_{v,c} = g_{m,RF}R_L$ where $g_{m,RF}$ is the transconductance of the lower transistors and R_L is the load resistance above the LO transistors. However the conversion becomes $\frac{g_{m,RF}R_L}{1+g_{m,RF}R_{RF}}$ with degeneration which is small for large $g_{m,RF}R_{RF}$. We assumed that the ADC would have a high impedance and did not load the mixer beyond the gain driven loading resistors, however if the impedance was non-negligible the transconductance and resistor values would need to be reconsidered.

D. Delay Line Design

The Delay Line was designed to mimic the signal propagation from the transmit to receive antenna and provide a way

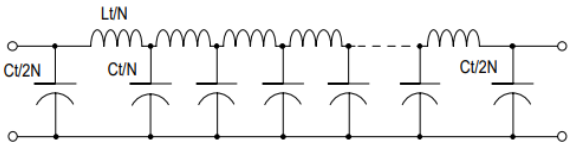

FIG. 6. **Delay Line Topology** This diagram shows the topology used as a lumped element transmission line.[4]

TABLE V. Delay Line Specifications

Specification	Desired	Achieved
Attenuation at 27GHz	2dB±0.5dB	2.088dB
Attenuation Ripple Over Band	<0.2dB	0.187dB
Delay at 27GHz	3ps±0.1ps	3.05ps
Bandwidth	50GHz	105GHz

for digital processing to gate out that leakage. The two important specifications for this line are the attenuation, which should match free space path loss from the transmit to receive antenna, and the time delay generated by the delay line at the center of our band. We assumed our transmit and receive antenna were 1mm apart, which is a reasonable assumption given they are low power and can be placed on chip. This distance corresponds to 3ps at 27GHz. We also assumed both antenna had a gain of 2dB, which is a typical value for a half-wave dipole[3], and using the Friis transmission equation, we find an attenuation of 2dB. We decided to use a lumped element transmission line model with Zo = 50 in order to generate this delay. Several important equations used to design the line are shown below.

Delay Line Equations[4]

$$\text{Delay time: } \tau_d = \sqrt{L_t C_t}$$

$$\text{Characteristic Impedance: } Z_0 = \sqrt{\frac{L_t}{C_t}}$$

$$\text{Bandwidth: } BW = \frac{0.35}{\tau_r}$$

$$\text{Number of stages: } N = \left(\frac{\tau_d}{\tau_r}\right)^{1.36}$$

Given we want a delay time of 3ps, a characteristic impedance of 50 Ohms to match the rest of our system, and a bandwidth of at least 50GHz, we compute that a 1 stage line is sufficient, with $C_t = 66\,\text{fF}$, and $L_t = 16.6\,\text{nH}$.

The most challenging part of the delay line was using a real inductor and attempting to optimize its size.

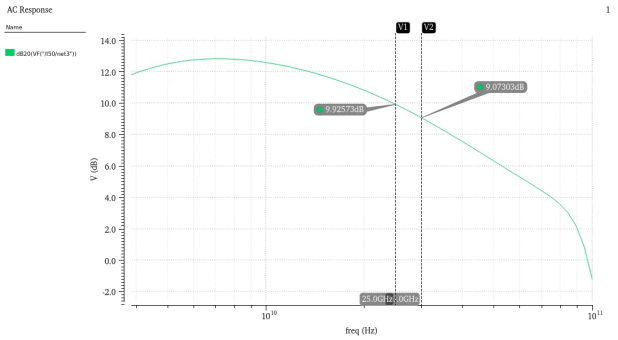

FIG. 7. **LNA AC Gain** This plot shows the small signal gain of the LNA over frequency.

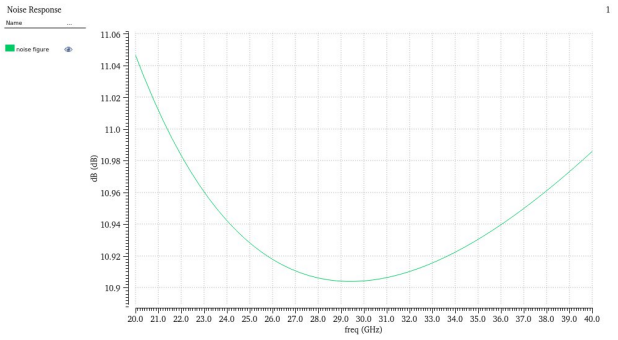

FIG. 8. **LNA NF Simulation** This plot shows the simulated NF of the LNA.

V. CADENCE VIRTUOSO ADE SIMULATIONS

A. Low Noise Amplifier Simulations

Simulations of the LNA aimed to show that it provided sufficient gain with low enough NF. These simulations are included. During the design process, additional simulations were performed, such as DFTs, to ensure linearity of the stage. These simulations shown are the final performance with real components as well as when loaded by the buffer stage.

B. Power Amplifier Simulations

Simulations of the power amplifier centered around validating small signal gain and drive capability, as well as ensuring that the differential output to the mixer had minimal common mode. Simulations revealed the amplifier was within our specifications, and was able to drive above 10mW over our antenna while also loaded with the delay line and mixer. The gain over frequency can be seen in Fig. 9, and a transient simulation of the output onto our 50 Ohm load is shown in Fig. 10. Finally, a transient simulation of the differential outputs to the mixer is shown in Fig. 11, validating that we have near unity gain, and good inversion. The differential output is not perfect and will lead to degradation of the mixer performance due to the common mode present, likely decreasing feedthrough frequency

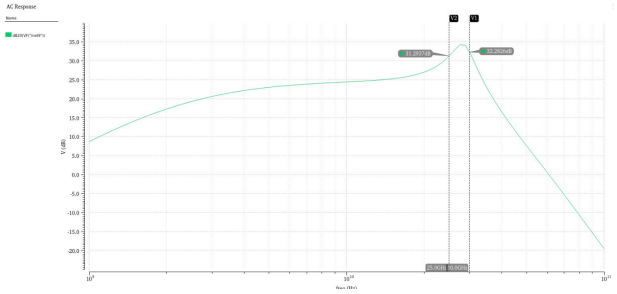

FIG. 9. **Power Amplifier AC Gain** This plot shows the small signal gain of the power amplifier over frequency.

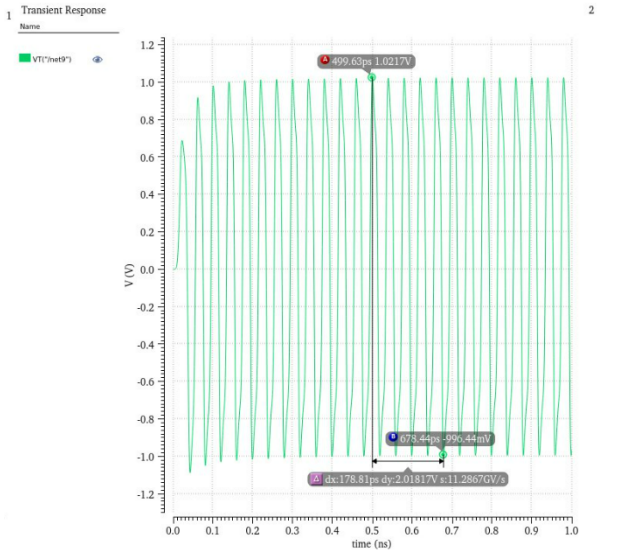

FIG. 10. **Power Amplifier Output Transient** This plot shows transient output from the Power Amplifier driven by a 50mV LO on a 50 Ohm Load

attenuation. However, this method is sufficient to meet our specifications.

C. Mixer Simulations

Once the mixer was put into cadence, the biasing became tricky as a single ended to differential converter was needed from the LNA to the mixer. We used an inverter with low gain to invert the signal and connect to the other RF input as a pseudo-differential input which worked well enough for our mixing but was not perfect (amplitudes were slightly off). Additionally, the LO waveforms were supplied by the power amplifier middle stages and there was some gain between them so they also were not the same amplitude. All of these factors somewhat affected the seen harmonics on the output, however there was still a factor of 10 separating the frequency presence of the down-converted signal and the harmonics for simulations of large frequency differences (25GHz and 30GHz) and small frequency differences (27.01 GHz and 27 GHz). See simulation results for details on the mixer performance within

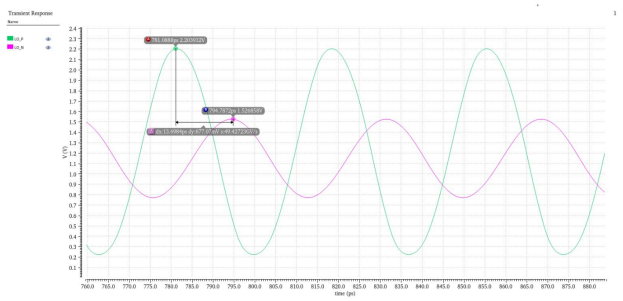

FIG. 11. **Power Amplifier Mixer Output Transients** This plot shows the positive and negative transients for the differential output of the Power Amplifier to the Mixer.

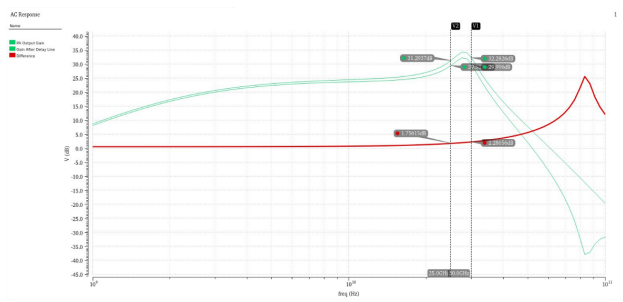

FIG. 12. **Delay Line AC Gain** This plot shows the small signal gain of the Delay Line over frequency.

the full system performance.

D. Delay Line Simulations

Simulations of the delay line were centered around validating AC gain across our band and time delay across our band. The gain across our band can be seen in Fig. 12, and a transient simulation of delay at 27GHz can be seen in Fig. 13.

E. Simulation Results

Overall, the system worked well together. In a simulation with a 27 GHz transmitter frequency and 27.01 GHz receiver frequency, the mixer produced a down-converted signal of 110 mV amplitude and 10 MHz frequency given a 50 mV amplitude input to the Power Amplifier and a 30 mV amplitude input to the LNA as seen in Fig. 14. As seen in Fig. 15, the LNA and the PA amplified these signals to 120 mV_{pp} and 2 V_{pp}, respectively. Lastly, the LNA output was mixed with separate outputs from the PA to down-convert the signal to a 10 MHz signal. The transient signal can be seen in Fig. 16 and its DFT can be seen in Fig. 17. A top level diagram of the system in Cadence Virtuoso can be seen in Fig. 18.

One interesting thing that we are not quite sure about is that in addition to the difference, sum, and feedthrough frequencies, we also see a very small amplitude at 3GHz, as well as 30GHz. We theorized that some external source to the mixer

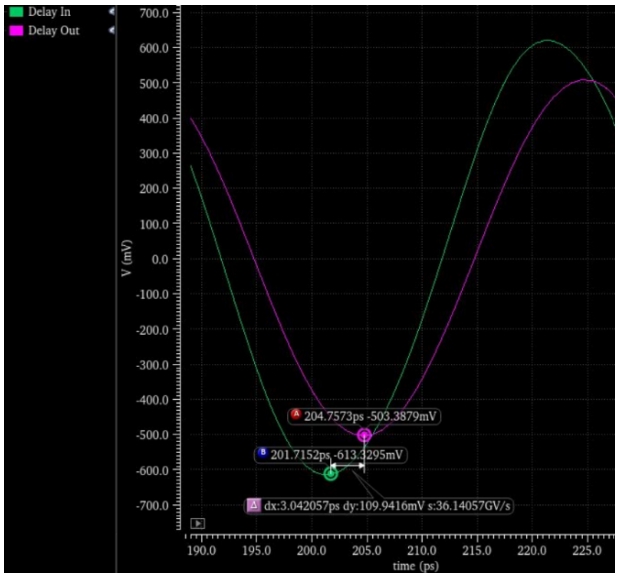

FIG. 13. **Delay Line Output Transient** This plot shows the transient output from the Delay Line given a 27GHz input signal from the Power Amplifier.

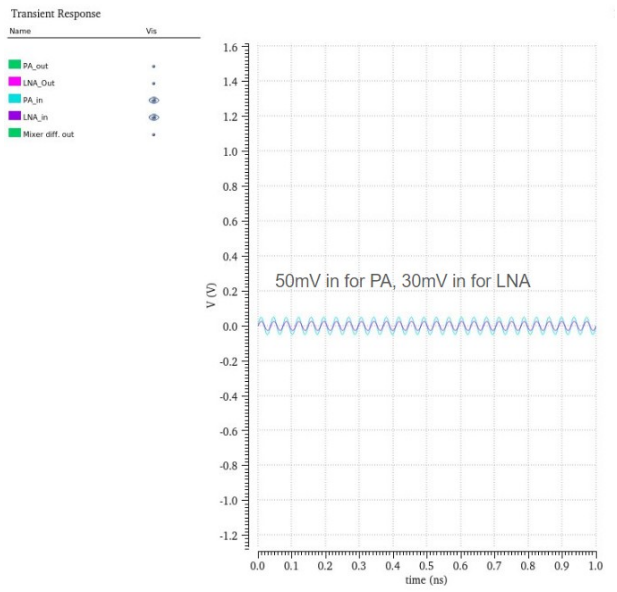

FIG. 14. **Input Signals for Full System Simulation** This plot shows the 27 GHz input to the PA and the 27.01 GHz input to the LNA

is generating 30GHz, which then mixes with 27GHz to provide a 3GHz signal, but we are not quite sure of the source. This signal does not interfere with our specifications as it is such low amplitude, but it is an interesting phenomenon, and would lead to a small distance error if the difference in transmit and receive frequencies is 3GHz.

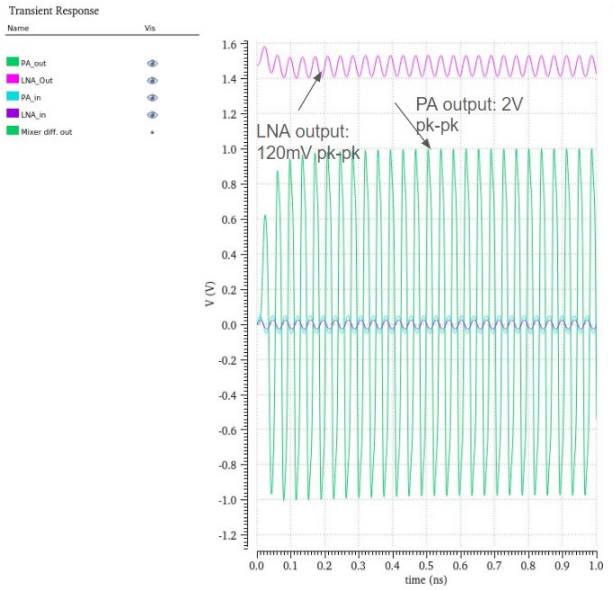

FIG. 15. **LNA and PA Signals for Full System Simulation** This plot shows the 27 GHz input to the PA and the 27.01 GHz input to the LNA

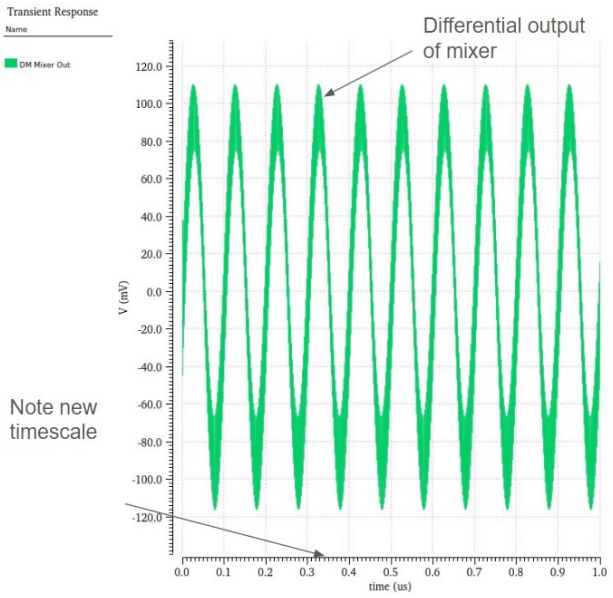

FIG. 16. **Mixer Output Transient for Full System Simulation** This plot shows the 100 MHz transient output of the mixer in the full simulation.

VI. FLOORPLAN AND LAYOUT

We did not finish layout and obtain DRC/LVS clean, but we did design a floorplan for the blocks as seen in Fig. 19. It emphasises minimum size while putting the transmit port and receive port on opposite sides of the chip to minimize leakage. Another thing we would do for the layout given more time is create via fencing between the transmit and receive path in order to reduce leakage. Our total expected size is 126um x

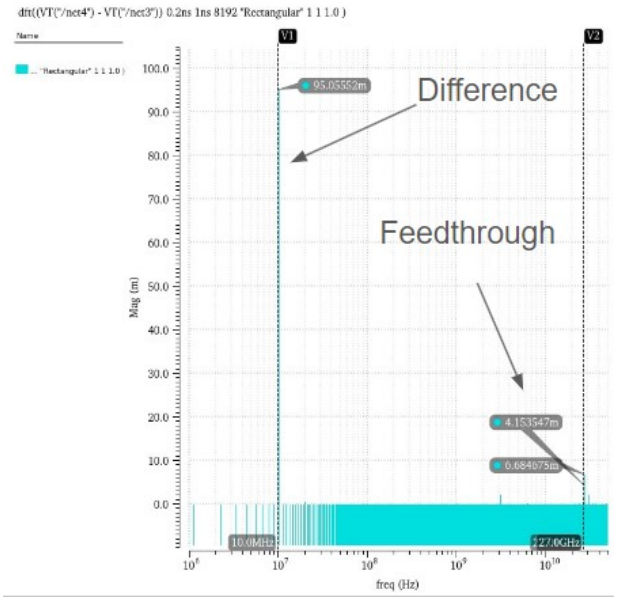

FIG. 17. **Mixer Output DFT for Full System Simulation** This plot shows the DFT of the output of the mixer in the full simulation, with the desired frequency difference and some low amplitude feedthrough.

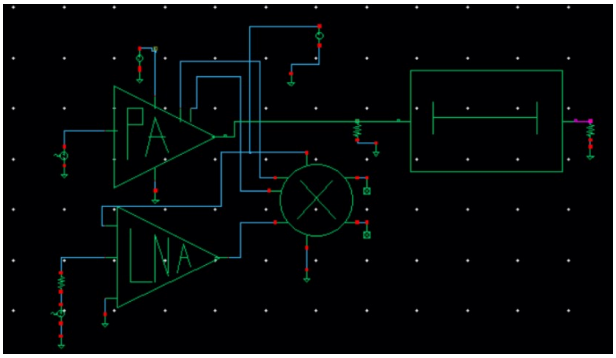

FIG. 18. **Top Level Schematic of the Transceiver** The Power Amplifier, Low Noise Amplifier, Mixer, and Delay Line connected in schematic, as well as their source or load impedances.

241um, or about 30 square millimiters.

VII. DISCUSSION AND CONCLUSIONS

A. Discussion

We have designed a FMCW Radar Transceiver that meets specifications but is quite inefficient. Additionally, there is some asymmetry in the mixer inputs which could be tuned for better harmonic suppression. The mixer RF input transistors degeneration, led the mixer to have a lower gain and presents an option for future development: switching to a passive mixer with an IF amplifier following it or modifying the topology of the current mixer to have higher gain in the desired frequency

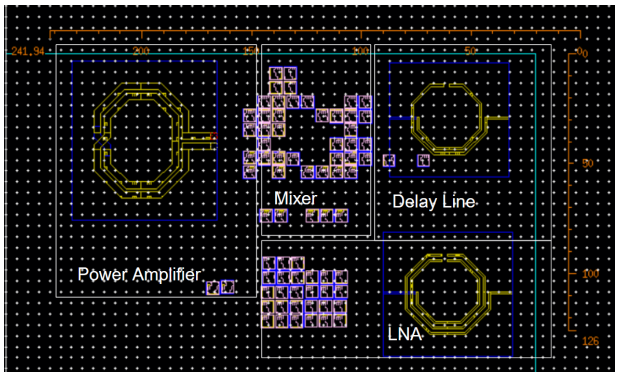

FIG. 19. **Layout Floorplan**

range. If there was more time within the project, specifications with the mixer could be better developed and validated, such as conversion gain over the frequency band of operation, as well as IIP3, input referred noise, and better designed gain.The simulations to characterize these specifications (Periodic Steady State Analysis and Quasi-Periodic Steady State Analysis) were discovered too late in the project timeline to implement and there was a larger focus on connecting the components together to get the system working fully.

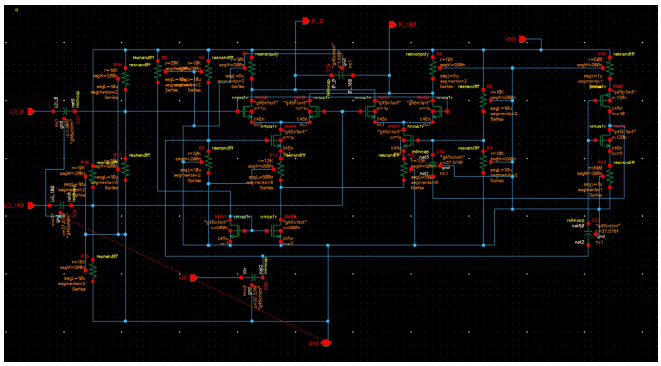

FIG. 20. **Mixer Schematic** Cadence Virtuoso implementation of the mixer

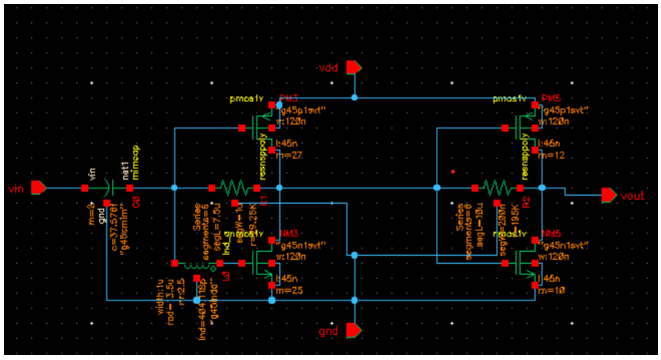

FIG. 21. **LNA Schematic** Cadence Virtuoso implementation of the LNA

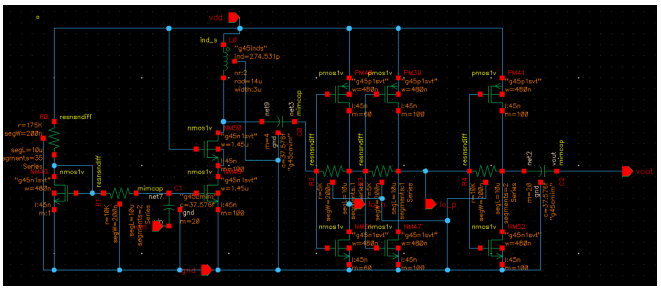

FIG. 22. **Power Amplifier Schematic** Cadence Virtuoso implementation of the PA

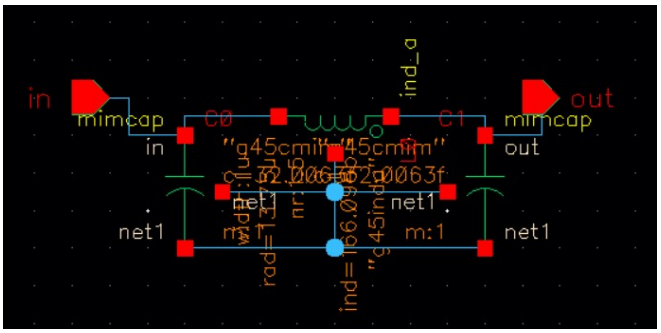

FIG. 23. **Delay Line Schematic** Cadence Virtuoso implementation of the Delay Line

B. Conclusion

This project gave our team a first glance into RF integrated circuit design which was somewhat out of the course scope, but managed to develop a design for an FMCW Radar Transceiver which passed key specifications. The power efficiency of the design was smaller than desired as was the gain of the active mixer. One valuable takeaway from this is first-hand experience as to why inductors aren't used as much as capacitors, as our layout is almost 50% inductors by area. This also allowed us to combine complicated blocks and taught us about how to design as a part of a larger system. We also learned that the process we are using does not model fingers correctly, which leads to inaccurate simulations when using many fingers.

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